module alu(clk,rst,sel,en\_rca,en\_cla,en\_csa,en\_sh);

input clk,rst;

input [2:0]sel;

output reg en\_rca,en\_cla,en\_csa,en\_sh;

always@(posedge clk)

begin

if(rst)

begin

en\_rca<=1'b0;en\_cla<=1'b0;en\_csa<=1'b0;en\_sh<=1'b0;

end

else

begin

case(sel)

3'b000:begin en\_rca<=1'b1;en\_cla<=1'b0;en\_csa<=1'b0;en\_sh<=1'b0; end

3'b001:begin en\_rca<=1'b0;en\_cla=1'b1;en\_csa<=1'b0;en\_sh<=1'b0; end

3'b011:begin en\_rca<=1'b0;en\_cla=1'b0;en\_csa<=1'b0;en\_sh<=1'b1; end

endcase

end

end

endmodule